REMARKS

Applicant concurrently files herewith an excess claim fee for one (1) independent claim.

Claims 1-16 have been canceled, thereby rendering moot the 35 U.S.C. § 102(b) rejection of claims 1-16 and the rejection for informalities to claims 1, 3-4, 6-7, 9-10, and 12-13.

Claims 17-35 are all the claims currently pending in the present Applications. Claims 17-32 have been added to claim additional features of the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

I. THE CLAIMED INVENTION

The claimed invention, as recited in claim 1, is directed to a liquid crystal display which that includes a light shielding film formed on a pixel board, a first insulating film formed on the light shielding film, a semiconductor layer formed on the first insulating film, a second insulating film, serving as a gate insulating film, formed on the semiconductor layer and the first insulating film, and a gate line formed on the second insulating film. The semiconductor layer comprises a source region, a drain region, a channel region and an LDD region.

The invention further includes contact holes for connecting the gate line with the light

shielding film that are formed on opposing sides of the channel region and the LDD region. A part of the gate line is filled up in the contact holes, and lengths of the contact holes are provided as at least a total length of the channel region and the LDD region.

Conventional liquid crystal display devices comprise dummy contact holes which are formed at both the sides of the light doped drain region. However, the contact holes do not reach the back side light shielding film, and thus a gap occurs between the back side light shielding film and each dummy contact hole. Therefore, the TFT cannot be perfectly shielded from light.

With the present invention, however, light incident to the TFT channel portion and the lightly doped drain (LDD) portion can be intercepted. Accordingly, the optical leakage current of the pixel TFT can be reduced, thereby preventing the reduction of the contrast due to the optical leakage current and the degradation in image quality due to flicker or other problems.

II. THE PRIOR ART REJECTION

THE MURAIDE '120 REFERENCE

Although Applicant canceled claims 1-16, thereby rendering the rejection to Muraide '120 and '121 moot, Applicant discusses the '120 reference, in light of new claims 17-35, below.

Applicant gratefully acknowledges the Examiner's indications that the present invention includes allowable subject matter over Muraide '120 regarding the differences between the width of the contact holes in the present invention as compared to the width of the nearby side of the semiconductor layer.

Muraide '120 clearly fails to disclose or suggest "contact holes for connecting said gate line with said light shielding film that are formed on opposing sides of said channel region and said LDD region, wherein a part of said gate line is filled up in said contact holes, and lengths of said contact holes are provided as at least a total length of said channel region and said LDD region," as described in claim 17 (emphasis Applicant's).

Further, Muraide '120 clearly fails to disclose or suggest "contact holes for connecting said gate line with said light shielding film that are formed on opposing sides of said LDD region, wherein a part of said gate line is filled up in said contact holes, and lengths of said contact holes are provided as at least a length of said LDD region," as recited in claim 18.

As viewed from a plan view in Figure 5, a non-limiting, preferred embodiment of the present invention illustrates the channel region covered with the contact holes 6, gate line 4 and the light shielding Film 3. Contact holes 6 are also positioned proximate to the LDD and channel regions, thereby increasing their effectiveness as light shields over the conventional devices. This combination is not disclosed in Muraide '120, therefore there is no teaching or suggesting of "at least said channel region is covered with said contact holes, said gate line, and said light shielding film," as recited in claim 19 and "said LDD region is covered with said contact holes and said light shielding film," as recited in claim 20.

Further, Muraide '120 clearly fails to teach or suggest contact holes, as described in claims 17 and 18, which extend beyond the lengths of the semiconductor layer. In the preferred embodiment illustrated in Figure 5, both ends of the length of contact holes 6 extending past each respective end of the LDD region 2 and/or channel region 1. Therefore, there is no teaching or suggestion of the contact holes "wherein the distal ends of the length of each contact hole extend beyond the distal ends of the total length of said channel region and

of each contact hole extend beyond the distal ends of the total length of said channel region and said LDD region.," as described in claim 31 (emphasis Applicant's).

Thus, turning to the exemplary language of claim 17, there is no teaching or suggestion of "*[a] liquid crystal display device, comprising:*

a light shielding film formed on a pixel board;

a first insulating film formed on said light shielding film;

a semiconductor layer formed on said first insulating film;

a second insulating film, serving as a gate insulating film, formed on said semiconductor layer and said first insulating film; and

a gate line formed on said second insulating film;

wherein said semiconductor layer comprises a source region, a drain region, a channel region and a lightly doped drain (LDD) region, and

contact holes for connecting said gate line with said light shielding film that are formed on opposing sides of said channel region and said LDD region,

wherein a part of said gate line is filled up in said contact holes, and lengths of said contact holes are provided as at least a total length of said channel region and said LDD region," (emphasis Applicant's).

III. FORMAL MATTERS AND CONCLUSION

Proposed drawing corrections to Figures 1-4 are submitted herewith to overcome the Examiner's objection. It is noted that Figs. 1-4 are designated by a legend --Related Art--, because the inventions of the structures of Figs. 1-4 (Japanese Patent Application No. Hei-11-109979 and Japanese Patent Application No. Hei-11-360973) were not disclosed in a

States.

In view of the foregoing, Applicant submits that claims 17-35, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 6/11/03

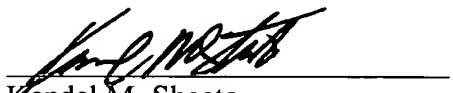

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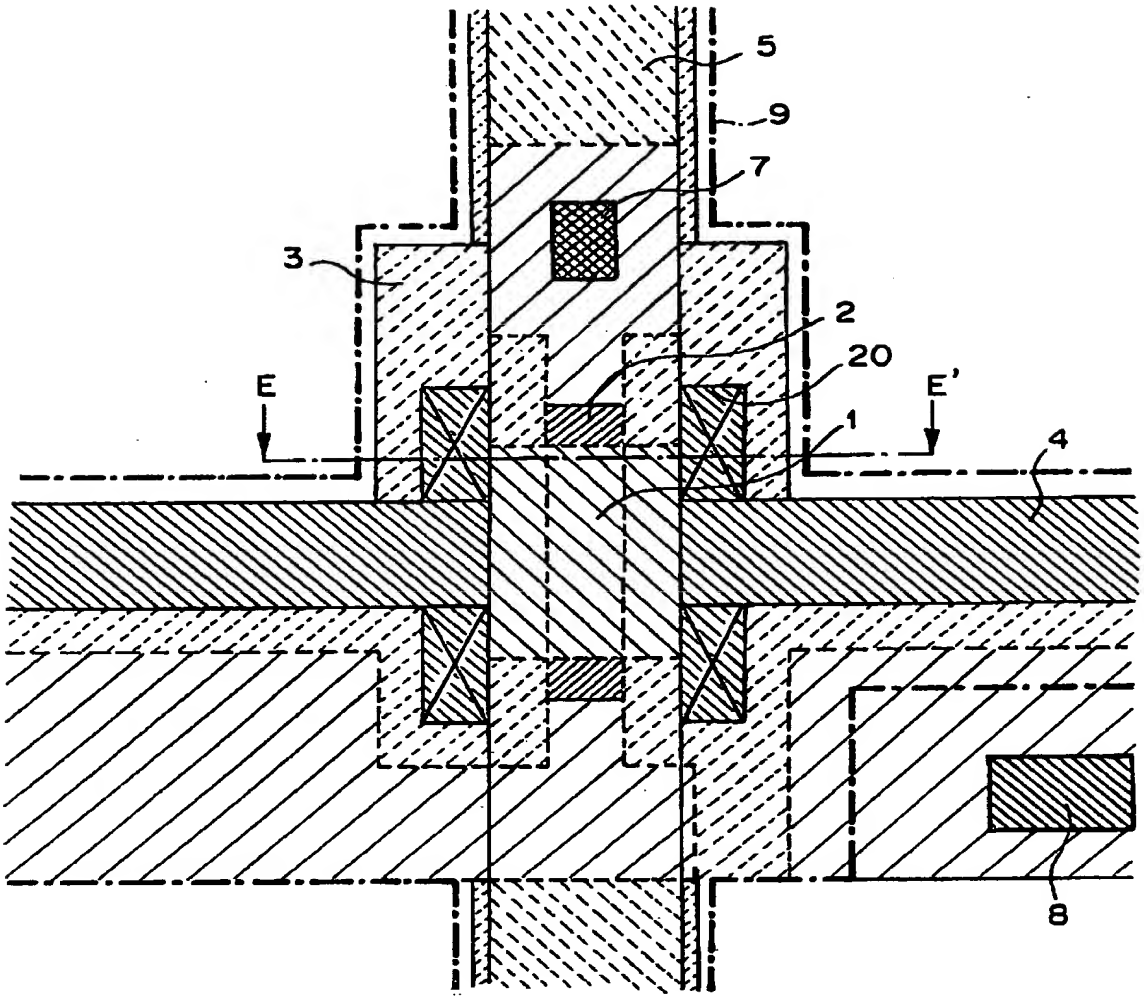
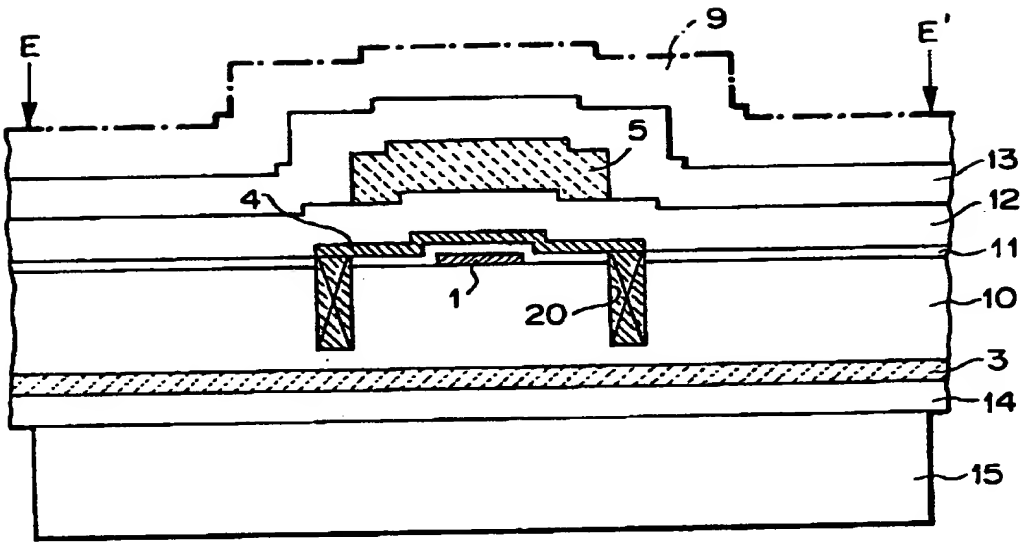
FIG. 1



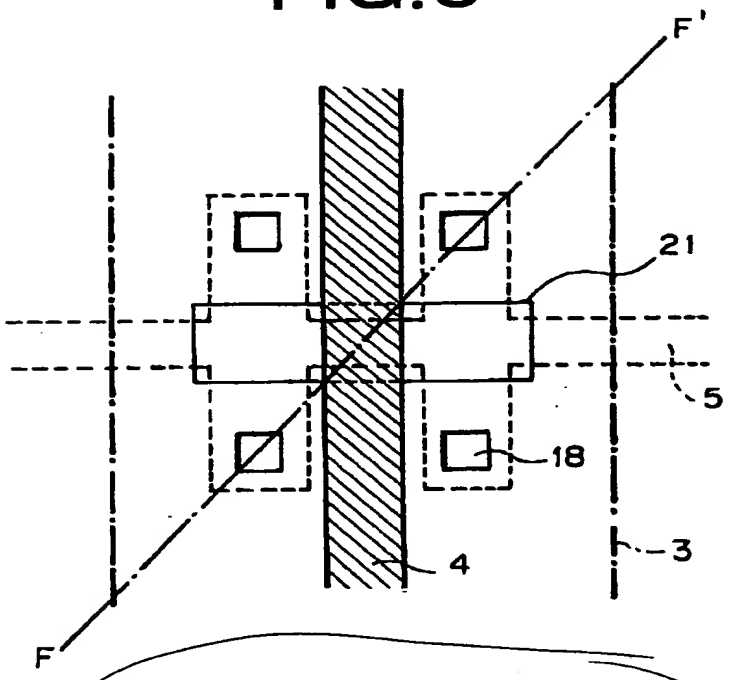
RELATED ART

FIG.2



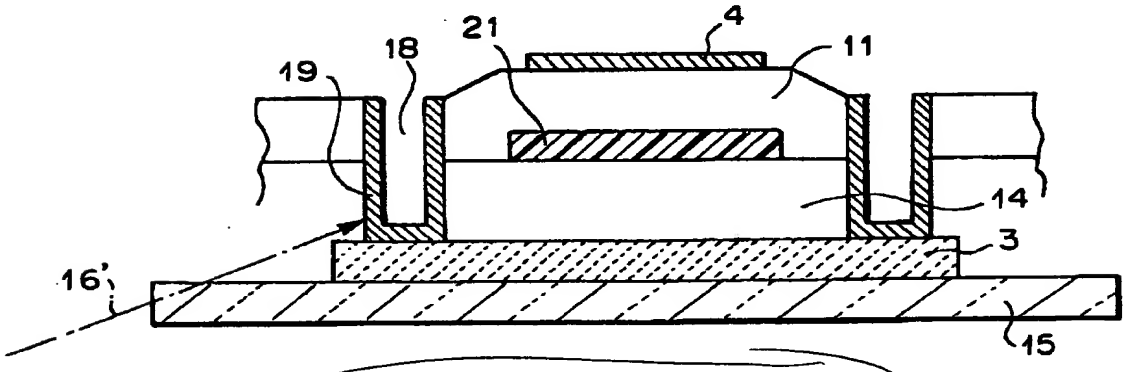
RELATED ART

FIG.3



RELATED ART

FIG.4



RELATED ART